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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KING, JUSTIN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 10/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,397	HEWITT ET AL.	
	Examiner	Art Unit	
	Justin I. King	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/22/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Moyer et al. (U.S. Patent No. 5,812,798).

Referring to claims 1 and 13: Moyer discloses that the CPU (figure 1, structure 12) dynamically determines the appropriate data bit width (column 2, lines 6-7) and then latches the data in the appropriate data bit width (column 2, lines 15-17). Moyer discloses the microprocessor adjusts the bit width (column 2, lines 12-21). Moyer discloses allocating the bus bit width and position in transmitting the data (column 3, lines 20-26). Moyer's microprocessor adjusting the bit width is equivalent to the claimed setting receive width; Moyer's allocating the bus bit width and position is equivalent to the claimed setting a transmit width; and Moyer's connecting means (microprocessor's interface to bus, the bus, and select register) between the microprocessor and external device is equivalent to the claimed link interface. Hence, claim is anticipated by Moyer.

Referring to claims 2, 10, and 14: Sine Moyer configures the CPU's bus width according to the I/O device's bus width, the transmit width is the lesser of the maximum of the CPU's transmit width and the maximum of the I/O device's transmit width.

Referring to claim 3: Moyer discloses the external device (column 2, line 9), which is equivalent to the external source.

Referring to claims 4, 11, and 15: Since the I/O device receives the data from the CPU via a bridge (figure 1, structure 22), the receive width is the lesser of the maximum of the I/O device's receive width and the maximum of the bridge and CPU's transmit width.

Referring to claims 5 and 16: Moyer discloses providing maximum receive width (column 2, lines 10-11) and providing a maximum transmit width (column 2, lines 17-19).

Referring to claims 6 and 17: Since Moyer's CPU configures the data width according to the I/O device's data width, the CPU's data width configuration is equivalent to the providing a CPU's maximum transmit width in determining the I/O device's usable receive width, and the bridge provides a maximum receive width in determining the received usable width.

Referring to claim 7: Moyer discloses that CPU attempts with a default bus width during the first bus cycle (column 2, lines 14-15), which is equivalent to the setting the transmit width to a default value. Moyer discloses that the data port size (DSZ) is initialized (column 13, lines 18-20), which is equivalent to the setting the receive width to a default value.

Referring to claims 8-9: Claims are rejected as the claim 1's argument stated above; furthermore, Moyer discloses that the CPU configures the maximum transmit width according to the I/O device's response (column 2, lines 15-19), the means for configuring the transmit width is equivalent the claimed transmit controller and the programmable transmit width register. Moyer discloses a control circuitry (figure 2, structure 102), decode logic (figure 2, structure 105), and control register (figure 2, structure 94) to hold the data port size and to control the bus

width (column 5, lines 5-10, column 11, first paragraph). The data port size (DSZ) value is the programmable receive width indicating the physical width.

Referring to claim 12: Moyer discloses that the CPU configures the maximum transmit width according to the I/O device's response (column 2, lines 15-19), the means for configuring the transmit width is equivalent the claimed maximum transmit width register. Moyer discloses control register to hold the data port size and to control the bus width (column 5, lines 5-10, column 11, first paragraph). The data port size (DSZ) value is the maximum receive width indicating the physical width.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Aldereguia et al. (U.S. Patent 5,255,374) and Moyer.

Referring to claims 1 and 13: Aldereguia discloses an operation of system bus and I/O bus via a bus interface unit/bridge (column 2, lines 36-69, column 3, lines 1-20). Aldereguia discloses that the data bus width of the system device is greater than the data bus width of the I/O device (column 2, lines 67-68). Aldereguia discloses buffering the data from the system device to the I/O device (column 3, lines 9-12). Aldereguia discloses that it is known to accommodate the different bus width between the I/O device and system device, but Aldereguia does not disclose setting the transmit width or receive width to accommodate the different bus width. Since the bridge connects to different I/O devices with different bus width, each data transmission between the bridge and a particular I/O device is set to the bus width according to that particular I/O device's data width, which is equivalent to the claimed setting a receive width.

Moyer discloses that the CPU dynamically determines the appropriate data bit width (column 2, lines 6-7) and then latches the data in the appropriate data bit width (column 2, lines 15-17). Moyer teaches one to seamlessly transfer the data between two different data bus width without buffering. Moyer's latching data according to appropriate bus bit width is the setting a transmit width based on a usable transmit width. Moyer discloses the microprocessor adjusts the bit width (column 2, lines 12-21). Moyer discloses allocating the bus bit width and position in transmitting the data (column 3, lines 20-26). Moyer's microprocessor adjusting the bit width is equivalent to the claimed setting receive width; Moyer's allocating the bus bit width and position is equivalent to the claimed setting a transmit width; and Moyer's connecting means (microprocessor's interface to bus, the bus, and select register) between the microprocessor and external device is equivalent to the claimed link interface.

Hence, it would have been obvious to one having ordinary skill in the computer art to adapt Moyer's teaching onto Aldereguia because Moyer teaches one establish a bufferless data transmission by dynamically configuring the processor to different bus sizes.

Referring to claims 2, 10, and 14: Sine Moyer configures the CPU's bus width according to the I/O device's bus width, the transmit width is the lesser of the maximum of the CPU's transmit width and the maximum of the I/O device's transmit width.

Referring to claim 3: Moyer discloses the external device (column 2, line 9), which is equivalent to the external source.

Referring to claims 4, 11, and 15: Since the I/O device receives the data from the CPU via a bridge (figure 1, structure 22), the receive width is the lesser of the maximum of the I/O device's receive width and the maximum of the bridge and CPU's transmit width.

Referring to claims 5 and 16: Moyer discloses providing maximum receive width (column 2, lines 10-11) and providing a maximum transmit width (column 2, lines 17-19).

Referring to claims 6 and 17: Since Moyer's CPU configures the data width according to the I/O device's data width, the CPU's data width configuration is equivalent to the providing a CPU's maximum transmit width in determining the I/O device's usable receive width, and the bridge provides a maximum receive width in determining the received usable width.

Referring to claim 7: Moyer discloses that CPU attempts with a default bus width during the first bus cycle (column 2, lines 14-15), which is equivalent to the setting the transmit width to a default value. Moyer discloses that the data port size (DSZ) is initialized (column 13, lines 18-20), which is equivalent to the setting the receive width to a default value.

Referring to claims 8-9: Claims are rejected as the claim 1's argument stated above; furthermore, Moyer discloses that the CPU configures the maximum transmit width according to the I/O device's response (column 2, lines 15-19), the means for configuring the transmit width is equivalent the claimed transmit controller and the programmable transmit width register. Moyer discloses a control circuitry (figure 2, structure 102), decode logic (figure 2, structure 105), and control register (figure 2, structure 94) to hold the data port size and to control the bus width (column 5, lines 5-10, column 11, first paragraph). The data port size (DSZ) value is the programmable receive width indicating the physical width.

Referring to claim 12: Moyer discloses that the CPU configures the maximum transmit width according to the I/O device's response (column 2, lines 15-19), the means for configuring the transmit width is equivalent the claimed maximum transmit width register. Moyer discloses control register to hold the data port size and to control the bus width (column 5, lines 5-10, column 11, first paragraph). The data port size (DSZ) value is the maximum receive width indicating the physical width.

Response to Arguments

6. In response to Applicant's argument that Applicant's claimed subject matter is **generally** directed to a communication link interface (Remark, page 9, first 2 lines), and Moyer address data bus load imbalance (Remark, page 9, 2nd paragraph): As the Specification disclosed, the alleged invention does address the problem of the bus loading (Specification, page 2, last paragraph).

7. In response to Applicant's argument that neither Moyer nor Aldereguia discloses setting both a transmit width of a transmit portion of a link interface and a receive width of a receive portion of the link interface (Remark, page 9, last paragraph, page 10, 2nd paragraph): Moyer discloses the microprocessor adjusts the bit width (column 2, lines 12-21). Moyer discloses allocating the bus bit width and position in transmitting the data (column 3, lines 20-26). Moyer's microprocessor adjusting the bit width is equivalent to the claimed setting receive width; Moyer's allocating the bus bit width and position is equivalent to the claimed setting a transmit width; and Moyer's connecting means (microprocessor's interface to bus, the bus, and select register) between the microprocessor and external device is equivalent to the claimed link interface.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 571-272-3628. The examiner can normally be reached on Monday through Friday, 9:00 am to 5:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3632 or on the central telephone number, (571) 272-2100. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

Justin King
September 29, 2005

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